THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today

- (1) was not written for publication in a law journal and
- (2) is not binding precedent of the Board.

Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte STEPHEN FLANNAGAN

Appeal No. 95-2433 Application $08/076,080^{1}$

REHEARING

Before KRASS, FLEMING, and LEE, <u>Administrative Patent Judges</u>.

KRASS, Administrative Patent Judge.

ON REQUEST FOR REHEARING

Appellant requests rehearing based on an alleged

Application for patent filed June 14, 1993. According to appellant, this application is a division of Application 07/951,620, filed September 28, 1992, now U.S. Patent No. 5,293,081, issued March 8, 1994, which is a division of Application 07/763,018, filed September 20, 1991, now U.S. Patent No. 5,184,033, issued February 2, 1993.

Application No. 08/076,080

overlooked point in our decision of June 17, 1998.

More particularly, appellant alleges that even if the substitutions alleged by the examiner are considered to have been obvious, the resulting structure still does not teach or suggest the limitations of claim 16. In support thereof, appellant submits five figures, starting from Fig. 2 of Nagano and changes one at a time, from PNP transistors substituted for NPN transistors, to reversal of power supply polarities to reversal of positive and negative power supplies and, finally, to a substitution of P-channel MOS transistors substituted for PNP transistors, resulting in Figure 5 in the request for rehearing. Appellant then points out that even if all of these changes were made to Nagano's circuit, the subject matter of claim 16 is still not reached.

Specifically, appellant cites the following differences:

- 1. Transistor Q3 does not have its source coupled to terminal \mathtt{OUT} .
- 2. Transistor Q3 does not have its drain coupled to a current mirror.
- 3. The circuit of Figure 5 in the request for rehearing does not function as a square-law clamping circuit.
 - 4. The current IO in resulting Figure 5 is completely

determined by currents I1 and I2 and the voltage on terminal OUT floats to a level which supplies IO under varying load conditions whereas the second MOS transistor of claim 16 has its source coupled to the I/O terminal. Accordingly, the current through the second MOS transistor will vary.

We are unpersuaded by appellant's arguments since appellant has derived a circuit (Figure 5 in the request for rehearing) completely by bodily incorporation of elements without considering the level of skill of the artisan in determining the obviousness of the instant claimed subject matter as a whole. One must look to what the art, as a whole, would have suggested to the skilled artisan and not merely to what a resulting circuit would look like by physically substituting one element for another in a sequential manner.

With regard to the first argument, transistor Q3 of Nagano has its collector, which is equivalent to the source of a MOS transistor, coupled to the terminal OUT.

With regard to the second argument, transistor Q3 of Nagano has its emitter, which is equivalent to the drain of a MOS transistor, coupled to current mirror circuit 11.

With regard to appellant's third argument, as we explained in our decision, at pages 4-5, while Nagano does

disclose an arithmetic operation circuit, this does not preclude the circuit, or part thereof, from operating in a clamping circuit manner. It would appear that the signal at the terminal OUT in Nagano is clamped to the voltage level generated from Q4 by transistor Q3, just as appellant's transistor 132 clamps output 100 to the voltage generated by transistor 135. This has been the examiner's position and, while that position appears quite reasonable to us, appellant has provided no argument thereagainst, other than to say that there is no clamping function in Nagano. Appellant has not provided any argument or evidence as to why terminal OUT in Nagano is not clamped to the voltage level generated from transistor O4 by transistor O3.

We also note, as we did at page 5 of our decision, that while appellant argues the "square-law clamping" aspect of the invention, this term appears only in the claim preamble and there is nothing within the body of the claim indicative of any "square-law clamping" or any clamping at all.

With regard to appellant's last argument relative to current IO in Nagano, it is not seen where this argument is

relevant to the claimed subject matter which recites a circuit structure but recites nothing about the current at terminal OUT.

We have considered appellant's request for rehearing and have granted the request to that extent but we deny the request

with respect to making any changes in our decision as we are unconvinced of any error therein.

DENIED

Errol A. Krass Administrative Patent Judge

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PATENT	Michael R. Fleming) BOARD OF
	Administrative Patent Judge) APPEALS AND) INTERFERENCES)
	Jameson Lee Administrative Patent Judge)

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